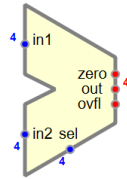

Arithmetic Logic Unit - Gate



An **arithmetic logic unit (ALU)** is a combinational digital circuit that performs arithmetic and bitwise operations.

The operation performed is selected by means of port *sel*. The output ports *zero* and *ovfl* (overflow) provide additional information about the result (*out*).

Port Name	Port Function
<i>in1, in2</i>	Logic: input words of bits Arithmetic: signed numbers
<i>out</i>	Logic: output word of bits Arithmetic: signed number
<i>sel</i>	Operation: see table below
<i>zero</i>	Zero flag: (HIGH/1) if result is zero valued
<i>ovfl</i>	Overflow flag for arithmetic operations

sel	Logical Function	sel	Arithmetic Function
0000	Bitwise AND	1000	Add
0001	Bitwise XOR	1001	Subtract
0010	Bitwise OR	1010	Reverse Subtract ($in2 - in1$)
0011	Bitwise NOT	1011	Multiply
0100	BIC – Bit Clear	1100	Increment $in1$
		1101	Decrement $in1$
		1110	$out := in1$
		1111	$out := in2$

Property	Settings	Meaning
Input Bits	Standard	Number of bits of input words
Output Bits	Standard	Number of bits of output word <i>out</i>
Delay	Delays	Propagation delay from each input port to output port <i>out</i> . $t_{pd} = t_{plh} = t_{phl}$
Rejection Limit	Delays	Inertial delay for all input ports. All signal spikes shorter than the rejection limit are canceled. This is called pulse rejection: $t_{pd} \geq t_{inertial}$
