

D-Flip-Flop Gate

The flip-flop is a basic building block of sequential logic circuits. It is a gate that has two stable states and can store one bit of state information.

The basic D-Flip-Flop has a D (data) input and a CLK (clock) input and outputs Q and \overline{Q} (the inverse of Q).

This flip-flop is positive edge-triggered. This means that the flip-flop changes output value only when the clock is at a positive edge (or rising clock edge).

Symbol	Truthtable												
	<table><tr><th>D</th><th>Clk</th><th>Q</th><th>\overline{Q}</th></tr><tr><td>0</td><td>↑</td><td>0</td><td>1</td></tr><tr><td>1</td><td>↑</td><td>1</td><td>0</td></tr></table>	D	Clk	Q	\overline{Q}	0	↑	0	1	1	↑	1	0
D	Clk	Q	\overline{Q}										
0	↑	0	1										
1	↑	1	0										

Property	Settings	Meaning
Clock-to-Q	Delays	The Clock-to-Q delay is the delay measured from clk 's rising edge to the output.
Setup-Time	Delays	Setup time is defined as the minimum amount of time before the clk 's rising edge by which the data D must be stable for it to be stored correctly. Any violation in this required time causes incorrect data to be captured and is known as a <i>setup violation</i> which may cause <i>metastability</i> of state and outputs.
