

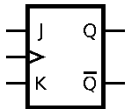
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## JK-Flip-Flop

The flip-flop is a basic building block of sequential logic circuits. It is a gate that has two stable states and can store one bit of state information.

This JK-Flip-Flop has  $J$  (set/jump) and  $K$  (reset/kill) inputs and a  $clk$  (clock) input and outputs  $Q$  and  $\overline{Q}$  (the inverse of  $Q$ ).

This flip-flop is positive edge-triggered. This means that the flip-flop changes output value only when the clock is at a positive edge (or rising clock edge).

Symbol	Truthtable																														
	<table><tr><th><math>J</math></th><th><math>K</math></th><th><math>clk</math></th><th><math>Q^*</math></th><th><math>\overline{Q}^*</math></th><th></th></tr><tr><td>0</td><td>0</td><td><math>\uparrow</math></td><td><math>Q</math></td><td><math>\overline{Q}</math></td><td>hold</td></tr><tr><td>0</td><td>1</td><td><math>\uparrow</math></td><td>0</td><td>1</td><td>reset/kill</td></tr><tr><td>1</td><td>0</td><td><math>\uparrow</math></td><td>1</td><td>0</td><td>set/jump</td></tr><tr><td>1</td><td>1</td><td><math>\uparrow</math></td><td><math>\overline{Q}</math></td><td><math>Q</math></td><td>toggle</td></tr></table> <p><math>Q</math>: current value <b>before</b> rising edge of <math>clk</math>. <math>Q^*</math>: next value <b>after</b> rising edge of <math>clk</math>.</p>	$J$	$K$	$clk$	$Q^*$	$\overline{Q}^*$		0	0	$\uparrow$	$Q$	$\overline{Q}$	hold	0	1	$\uparrow$	0	1	reset/kill	1	0	$\uparrow$	1	0	set/jump	1	1	$\uparrow$	$\overline{Q}$	$Q$	toggle
$J$	$K$	$clk$	$Q^*$	$\overline{Q}^*$																											
0	0	$\uparrow$	$Q$	$\overline{Q}$	hold																										
0	1	$\uparrow$	0	1	reset/kill																										
1	0	$\uparrow$	1	0	set/jump																										
1	1	$\uparrow$	$\overline{Q}$	$Q$	toggle																										

Property	Settings	Meaning
<b>Clock-to-Q</b>	Delays	The clock-to-Q delay is the delay measured from $clk$ 's rising edge to the output.
<b>Setup-Time</b>	Delays	Setup time is defined as the minimum amount of time <b>before</b> the $clk$ 's rising edge by which the inputs $J$ and $K$ must be stable for it to be stored correctly. Any violation in this required time causes incorrect data to be captured and is known as a <i>setup violation</i> which may cause <i>metastability</i> of state and outputs.

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