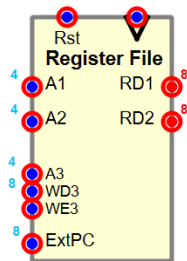

RegisterFile

The RegisterFile implements a set of registers which are asynchronously readable and synchronously written.

It provides 8, 16 or 32 internal registers with 8, 16 or 32 bit data width and can be configured for 1 to 4 for parallel asynchronous read operations and 1 to 4 parallel synchronous write operations.



The example on the left side provides 16 8-bit registers. Hence, all address ports have a data width of 4 bits and all data ports are 8 bits wide.

This RegisterFile provides two independent address ports (*A1*, *A2*) for asynchronous read operations and a single address port (*A3*) for writing.

Associated data ports are *RD1* and *RD2* for reading and *WD3* for writing, respectively. *WE3* selectively enables a write operation to register at address *A3* of value *WD3* on a rising edge of clock.

Input *Rst* asynchronously resets all register value to zero.

Property	Settings	Meaning
Size	CPU	Number of internal registers
Width	CPU	Width of register in bits
Rd-Add	CPU	Number of read ports
WD-Add	CPU	Number of write ports
PC-Reg	CPU	Ext: Program Counter(the upmost register) is NOT part of Registerfile Int: All registers included
R0 Val	CPU	any: Register <i>R0</i> may hold arbitrary values 0: <i>R0</i> is fixed to value zero
Delay	Delays	Propagation delay from each <i>Ax</i> to <i>RDx</i> .
Clk2Q:	Delays	The Clock-to-Q delay is the delay measured from <i>clk</i> 's rising edge to the output.
