


---

## Decoder

An **address decoder** is a binary **decoder** that has two or more inputs for address bits and one or more outputs for device selection signals. When the address for a particular device appears on the address inputs, the decoder asserts the selection output for that device.

The below is the truth table for a basic 1 to 2 line decoder where  $A$  is the address input and  $y_0$  and  $y_1$  are outputs. An enable ( $e$ ) input turns address decoding on and off. Enable ( $e$ ) is required to build address decoders for arbitrary address lengths from a set of basic decoders.

Symbol	Truthtable	Function																		
	<table><tr><th><math>e</math></th><th><math>A</math></th><th><math>y_0</math></th><th><math>y_1</math></th></tr><tr><td rowspan="2">0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td rowspan="2">1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr></table>	$e$	$A$	$y_0$	$y_1$	0	0	0	0	1	0	0	1	0	1	0	1	0	1	$\mathbb{B}^2 \rightarrow \mathbb{B}^2$ : $y_0 = en\overline{A}, y_1 = enA$
$e$	$A$	$y_0$	$y_1$																	
0	0	0	0																	
	1	0	0																	
1	0	1	0																	
	1	0	1																	

Property	Settings	Meaning
Size	Standard	2/4/8: $2^n$ ( $n = 1, 2, 3$ ) number of output lines with address lines $A_0$ to $A_{n-1}$ .
Delay	Delays	Propagation delay from $A_i$ and $e$ to each output, $t_{pd} = t_{plh} = t_{phl}$
Rejection Limit	Delays	Inertial delay for all inputs; all signal spikes shorter than the rejection limit are canceled. This is called pulse rejection: $t_{pd} \geq t_{inertial}$

---