


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## Register with Enable and asynchronous Reset

The register implements a set of D-Flipflops with *enable* and asynchronous *reset* which are connected in parallel and driven by a common clock line.

The Register has a *D* (data) input vector, a *clk* (clock) input, an *en* (enable) input and an *R* (reset) input and output vectors *Q* and  $\overline{Q}$  (the inverse vector of *Q*).

The register is positive edge-triggered. This means it changes output value only when the clock is at a positive edge (or rising clock edge) **and** the input *en* is active (HIGH/1) **and** the reset input *R* is inactive (LOW/0). An active *R* input immediately sets all bits of *Q* to LOW/0 independently (= asynchronously) from *clk*'s rising edges.

Symbol	Truthtable																				
	<table><tr><th><i>R</i></th><th><i>en</i></th><th><i>clk</i></th><th><i>Q</i>*</th><th><math>\overline{Q}</math>*</th></tr><tr><td>1</td><td>-</td><td>-</td><td><math>\vec{0}</math></td><td><math>\vec{1}</math></td></tr><tr><td>0</td><td>0</td><td>↑</td><td><i>Q</i></td><td><math>\overline{Q}</math></td></tr><tr><td>0</td><td>1</td><td>↑</td><td><i>D</i></td><td><math>\overline{D}</math></td></tr></table> <p><i>Q</i>: current value <b>before</b> rising edge of <i>clk</i>. <i>Q</i>*: next value <b>after</b> rising edge of <i>clk</i>. <math>\vec{0}</math>: 00...0 with length of <i>D</i> <math>\vec{1}</math>: 11...1 with length of <i>D</i></p>	<i>R</i>	<i>en</i>	<i>clk</i>	<i>Q</i> *	$\overline{Q}$ *	1	-	-	$\vec{0}$	$\vec{1}$	0	0	↑	<i>Q</i>	$\overline{Q}$	0	1	↑	<i>D</i>	$\overline{D}$
<i>R</i>	<i>en</i>	<i>clk</i>	<i>Q</i> *	$\overline{Q}$ *																	
1	-	-	$\vec{0}$	$\vec{1}$																	
0	0	↑	<i>Q</i>	$\overline{Q}$																	
0	1	↑	<i>D</i>	$\overline{D}$																	

Property	Settings	Meaning
<b>Data Bits</b>	Multi-Bit	Number of data bits of <i>D</i> , <i>Q</i> , $\overline{Q}$
<b>Clock-to-Q</b>	Delays	The Clock-to-Q delay is the delay measured from <i>clk</i> 's rising edge to outputs.
<b>Setup-Time</b>	Delays	Setup time is defined as the minimum amount of time <b>before</b> the <i>clk</i> 's rising edge by which the data <i>D</i> must be stable for it to be stored correctly. Any violation in this required time causes incorrect data to be captured and is known as a <i>setup violation</i> which may cause <i>metastability</i> of state and outputs.

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