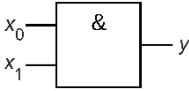

AND Gate

The **AND gate** is a basic digital gate with multiple inputs and a single output. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If none or not all inputs to the AND gate are HIGH, a LOW output results¹⁾. The AND gate implements the logical conjunction which is denoted as symbol \bullet , $\&$ or \wedge .

The gate shown below has two inputs x_0 and x_1 but can be extended to any number of inputs.

IEC Symbol	Truthtable	Function															
	<table><tr><th>x_1</th><th>x_0</th><th>y</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	x_1	x_0	y	0	0	0	0	1	0	1	0	0	1	1	1	$\mathbb{B}^2 \rightarrow \mathbb{B}: y = x_1 x_0$ $\mathbb{B}^2 \rightarrow \mathbb{B}: y = x_1 \cdot x_0$ $\mathbb{B}^2 \rightarrow \mathbb{B}: y = x_1 \wedge x_0$
x_1	x_0	y															
0	0	0															
0	1	0															
1	0	0															
1	1	1															

Property	Settings	Meaning
Inputs	Standard	Number of inputs (x_0 to x_{n-1})
Data Bits	Multi-Bit	Number of bits per input = Number of bits of output
Delay	Delays	Propagation delay from each x_i to y , $t_{pd} = t_{plh} = t_{phl}$
Rejection Limit	Delays	Inertial delay for all inputs x_i All signal spikes shorter than the rejection limit are canceled. This is called pulse rejection: $t_{pd} \geq t_{inertial}$

¹⁾ <https://en.wikipedia.org>
