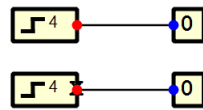

ClkGen – Clock Generator Gate



A ClkGen is used to produce a symmetric clock signal for stimulating e.g. flipflops during simulation runs.

While a simulation is running

- a left mouse click stops or restarts the generator. A stopped generator shows a black cross at its output port (see lower gate in the above Figure).
- a right mouse click opens a context menu which allows to define the cycle period. Stopping or pausing the simulation is not required for this.

| Property | Settings | Meaning |
|---------------------|----------|---|
| Clock Period | Standard | A period of length 4 (as shown above) produces a signal edge every two simulation ticks. A rising edge occurs every four ticks. |