

D-Latch Gate

The flip-flop is a basic building block of sequential logic circuits. It is a gate that has two stable states and can store one bit of state information.

The D-Latch has a D (data) input and a C (clock) input and outputs Q and \overline{Q} (the inverse of Q).

This flip-flop is level-triggered. This means that the flip-flop changes output value only when the clock is high.

The D-Latch is used to capture, or 'latch' the logic level which is present on the D line when the C input is high. If the data on the D line changes state while C is high, then the output, Q , follows the input, D . When the C input falls to logic 0 (falling edge), the last state of the D input is trapped and held in the latch¹⁾.

Symbol	Truthtable																							
	<table><tr><th>C</th><th>D</th><th>Q^*</th><th>$\overline{Q^*}$</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>Q</td><td>\overline{Q}</td><td rowspan="2">hold</td></tr><tr><td>0</td><td>1</td><td>Q</td><td>\overline{Q}</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="2">transparent</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td></tr></table> <p>Q: current value Q^*: next value</p>	C	D	Q^*	$\overline{Q^*}$	Mode	0	0	Q	\overline{Q}	hold	0	1	Q	\overline{Q}	1	0	0	1	transparent	1	1	1	0
C	D	Q^*	$\overline{Q^*}$	Mode																				
0	0	Q	\overline{Q}	hold																				
0	1	Q	\overline{Q}																					
1	0	0	1	transparent																				
1	1	1	0																					

Property	Settings	Meaning
Clock-to-Q	Delays	The Clock-to-Q delay is the delay measured from C 's falling edge to the output. For a D-Latch it is also the delay from D to Q in transparent mode ($C=1$).
Setup-Time	Delays	Setup time is defined as the minimum amount of time before the C 's falling edge by which the data D must be stable for it to be stored correctly. Any violation in this required time causes incorrect data to be captured and is known as a <i>setup violation</i> which may cause <i>metastability</i> of state and outputs.

¹⁾ vlab.amrita.edu
