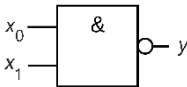

NAND Gate

The **NAND gate (NOT-AND)** is a basic digital gate with multiple inputs and a single output. A LOW (0) output results only if all the inputs to the gate are HIGH (1); if any input is LOW (0), a HIGH (1) output results. The NAND gate is significant because any boolean function can be implemented by using a combination of NAND gates. This property is called functional completeness¹⁾.

The gate shown below has two inputs x_0 and x_1 but can be extended to any number of inputs.

IEC Symbol	Truthtable	Function															
	<table><tr><th>x_1</th><th>x_0</th><th>y</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	x_1	x_0	y	0	0	1	0	1	1	1	0	1	1	1	0	$\mathbb{B}^2 \rightarrow \mathbb{B}: y = \overline{x_1 x_0}$ $\mathbb{B}^2 \rightarrow \mathbb{B}: y = \overline{x_1 \cdot x_0}$ $\mathbb{B}^2 \rightarrow \mathbb{B}: y = \neg(x_1 \wedge x_0)$
x_1	x_0	y															
0	0	1															
0	1	1															
1	0	1															
1	1	0															

Property	Settings	Meaning
Inputs	Standard	Number of inputs (x_0 to x_{n-1})
Data Bits	Multi-Bit	Number of bits per input = Number of bits of output
Delay	Delays	Propagation delay from each x_i to y , $t_{pd} = t_{plh} = t_{phl}$
Rejection Limit	Delays	Inertial delay for all inputs x_i All signal spikes shorter than the rejection limit are canceled. This is called pulse rejection: $t_{pd} \geq t_{inertial}$

¹⁾ <https://en.wikipedia.org>
