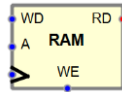

RAM – Random-Access Memory



Random-access memory is a form of memory that can be read and changed in any order. RAM implements a static memory of bytes, halfwords (16 bits) or words (32 bits). Little and big endianness byte order is available.

The memory has *WD* (data) and an *A* (address) input vectors, a *clk* (clock) input, a *WE* (write enable) input and an output vector *RD*.

The **write operation** is positive edge-triggered. This means memory content at address *A* is changed to data value *WD* only when the clock is at a positive edge (or rising clock edge) **and** the input *WE* is active.

Reading is performed asynchronously: Changing the address *A* when *WE* is (LOW/0) outputs the addressed memory content at the *RD* port.

Property	Settings	Meaning
A-Bits		Number of address bits: defines the size of memory elements
Bytes		1/2/4: Byte (8 bit), Halfword (16 bit), Word (32 bit)
Endianness		Big/Little: Endianness indicates the ordering of bytes within a multi-byte number.
Alignment		Yes: <i>Address</i> modulo <i>Bytes</i> must be 0.
Clk-to-Q	Delays	The Clock-to-Q delay is the delay measured from <i>clk</i> 's rising edge to outputs.
Setup-Time	Delays	Setup time is defined as the minimum amount of time before the <i>clk</i> 's rising edge by which the data <i>WD</i> must be stable for it to be stored correctly. Any violation in this required time causes incorrect data to be captured and is known as a <i>setup violation</i> which may cause <i>metastability</i> of state and outputs.